

CLAIMS

- 1 1. A method of forming a pitcher-shaped active area structure for a field effect
2 transistor (FET), the method comprising the steps of:
3 forming divots into top portions of side walls of at least two shallow trench insulator
4 (STI) structures formed into a substrate and that isolate a FET and define an
5 active area structure; and
6 migrating substrate material into at least portions of the divots, thereby forming a
7 widened top portion of the active area structure with a larger width than a
8 bottom portion of the active area structure.
- 1 2. The method of claim 1, wherein the step of forming divots into top portions of side
2 walls of at least two STI structures comprises the step of implementing a wet etch to
3 remove the top portions of the sidewalls of the at least two STI structures, thereby
4 forming divots in the top portions of the sidewalls of the at least two STI structures.
- 1 3. The method of claim 1, wherein the step of migrating substrate material into at least
2 portions of the divots comprises the step of implementing a hydrogen annealing
3 technique to migrate substrate material into at least portions of the divots, thereby
4 forming a widened top portion of the active area structure with a larger width than a
5 bottom portion of the active area structure.
- 1 4. The method of claim 3, wherein the step of implementing a hydrogen annealing
2 technique to migrate substrate material into at least portions of the divots further
3 comprises the step of rounding top corners of the widened top portion of the active
4 area structure.

- 1 5. A method of forming a pitcher-shaped active area structure for a field effect
2 transistor (FET), the method comprising:
3 implementing a wet etch to remove a pad oxide layer formed on a substrate and
4 portions of an STI oxide fill and STI liner oxide that form top portions of
5 sidewalls of at least two shallow trench insulator (STI) structures that isolate
6 a FET and define an active area structure, thereby forming divots in the top
7 portions of the sidewalls of the at least two STI structures; and
8 implementing a hydrogen annealing technique to migrate substrate material into at
9 least portions of the divots, thereby forming a widened top portion of the
10 active area structure with a larger width than a bottom portion of the active
11 area structure.
- 1 6. The method of claim 5, wherein the step of implementing a wet etch comprises the
2 step of implementing a buffered hydrogen fluoride acid (BHF) etch to remove the
3 pad oxide layer and portions of the STI oxide fill and the STI liner oxide that form
4 the top portions of the sidewalls of the at least two STI structures, thereby forming
5 divots in the top portions of the sidewalls of the at least two STI structures.
- 1 7. The method of claim 5, wherein the step of implementing a wet etch comprises the
2 step of implementing an isotropic plasma etch to remove the pad oxide layer and
3 portions of the STI oxide fill and the STI liner oxide that form the top portions of
4 the sidewalls of the at least two STI structures, thereby forming divots in the top
5 portions of the sidewalls of the at least two STI structures.
- 1 8. The method of claim 5, wherein the step of implementing a wet etch is performed
2 with a 40/1 etch chemistry and in the range of approximately 1 to 2 minutes.

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- 1 9. The method of claim 5, wherein the step of implementing a wet etch forms divots
2 with a depth of approximately 500 Å or less.
- 1 10. The method of claim 5, wherein the step of implementing a hydrogen annealing
2 technique to migrate substrate material into at least portions of the divots further
3 comprises the step of rounding top corners of the widened top portion of the active
4 area structure.
- 1 11. The method of claim 5, wherein the step of implementing a hydrogen anneal is
2 performed at a temperature of 700°C. or higher.
- 1 12. The method of claim 5, wherein the step of implementing a hydrogen anneal is
2 performed under a pressure of 10^{-3} Torr or higher.
- 1 13. A pitcher-shaped active area structure for a field effect transistor (FET) comprising:
2 a semiconductor substrate; and
3 at least two shallow trench insulator (STI) structures formed into the substrate that
4 isolate the FET and define an active area structure, the active area structure
5 comprising:
6 a widened top portion; and
7 a bottom portion, wherein the widened top portion has a larger width than
8 the bottom portion.
- 1 14. The structure of claim 13 further comprising a pad oxide layer formed on the
2 substrate, and wherein the at least two STI structures are formed into the substrate
3 through the pad oxide layer, the at least two STI structures comprising an STI oxide
4 liner and an STI oxide fill formed on the STI oxide liner.

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1 15. The structure of claim 13, wherein the at least two STI structures comprise divots in
2 top portions of side walls of the at least two STI structures into which the widened
3 top portion of the active area structure extends.

1 16. The structure of claim 15, wherein the semiconductor substrate comprises silicon,
2 and wherein the widened top portion formed into divots comprises single crystalline
3 silicon.

1 17. The structure of claim 15, wherein the divots comprise a depth of approximately
2 500 Å or less.

1 18. The structure of claim 13, wherein the widened top portion of the active area
2 structure further comprises rounded top corners.

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